REMARKS/ARGUMENTS

Claims 1-25 are pending in the present application. Claims 1, 2, 8, 12, 16, 19 and 23 were amended. No claims were added or canceled. Applicants believe claims 1-25 patentably distinguish over the cited art and that this case is now in condition for allowance. Reconsideration of the rejection is, accordingly, respectfully requested in view of the above amendments and the following comments.

I. 35 U.S.C. § 132(a)

The Examiner has objected to the Amendment filed May 2, 2006 under 35 U.S.C. § 132(a) as introducing new matter into the disclosure as a result of the deletion of the disclosure of transmission-type media on pages 64-65, and has required that the new matter be canceled.

By the present Amendment, the deleted subject matter has been reinstated into the specification. Therefore, the objection to the amendment filed May 2, 2006 under 35 U.S.C. § 132(a) has been overcome.

II. 35 U.S.C. § 101

The Examiner has rejected claims 19-25 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. This rejection is respectfully traversed.

In order to overcome this rejection, the Examiner suggests amending the claims to read "A computer program product in a computer readable recordable-type medium...". By the present Amendment, independent claims 19 and 23 have been so amended. Claims 19-25 are now believed to fully comply with the requirements of 35 U.S.C. § 101 and withdrawal of the rejection thereunder is respectfully requested.

III. 35 U.S.C. § 102, Anticipation

The Examiner has rejected claims 1-25 under 35 U.S.C. § 102(a) as being anticipated by Davidson et al. (U.S. Patent No. 6,574,727 B1). This rejection is respectfully traversed.

In rejecting the claims, the Examiner states as follows:

> As per claim 1, Davidson discloses a method in a data processing system for monitoring processing of instructions, the method comprising:
>
> receiving an instruction at a processor for execution; (Col. 8 lines 58-60)
>
> responsive to a determination of being in an enabled state to perform a selected action, (Col. 11, lines 35-55) *The examiner asserts that the "OK to Sample Signal" (Fig. 6 signal 642) indicates that the processor is in an enabled state to perform an action specified by the MMCR.*

> determining whether the instruction is associated with an indicator stored in a shadow memory; (Col. 8, line 65 – col. 9 line 8), the shadow memory comprising a storage area separate from an instruction storage area in which the instruction is stored; *The examiner asserts that the value to be matched is stored in the MMCR, as described in col. 4 line 9 – col. 5 line 30. Since the MMCR is implemented as a register on chip (col. 4 line 21), the value to be compared to is NOT stored in an instruction storage area and, hence, constitutes shadow memory.*
>
> and performing a selected action in response to the indicator being associated with the instruction. (Col. 8 lines 30-36)

Final Office Action dated May 31, 2006, page 3.

The present Amendment amends the independent claims 1, 8, 12, 16, 19 and 23 to define the "shadow memory" recited therein with greater specificity. Support for the amendments can be found, for example, on page 25, line 10 to page 26, line 23 and on page 38, line 21 to page 40, line 4. During a telephone interview on April 19, 2006, the Examiner agreed that Davidson could be overcome by amending the claims in such a manner; and Applicants believe the present Amendment emphasizes important differences between the MMCR in Davidson and the shadow memory of the present invention, and places the application in condition for allowance.

Claim 1 as amended herein is as follows:

> 1. A method in a data processing system for monitoring processing of instructions, the method comprising:
>
> receiving, from an instruction storage area storing instructions, an instruction at a processor for execution;
>
> responsive to a determination of being in an enabled state to perform a selected action, determining whether the instruction is associated with a performance indicator stored in a shadow memory, the shadow memory comprising a storage area separate from the instruction storage area and storing performance indicators associated with instructions stored in the instruction storage area; and
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> performing the selected action if a performance indicator is associated with the instruction.

Applicants respectfully submit that Davidson does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to amended claim 1, in particular, Davidson does not teach or suggest "responsive to a determination of being in an enabled state to perform a selected action, determining whether the instruction is associated with a performance indicator stored in a shadow memory, the shadow memory comprising a storage area separate from the instruction storage area and storing performance indicators associated with instructions stored in the instruction storage area", and "performing the selected action if a performance indicator is associated with the instruction".

Davidson is directed to a mechanism for selecting an instruction to be monitored within a pipelined processor. In particular, Davidson discloses that when instructions are fetched, they are matched against at least one match condition to generate instructions that are eligible for sampling. The instructions eligible for sampling are then sampled to generate sampled instructions, and the sampled instructions are marked in order that they may be monitored while executing within the pipelined processor. Col. 8, line 65-col. 9, line 8 referred to by the Examiner in rejecting the claims reads as follows:

> Instruction match facility **604** may be used to identify instructions by their opcode and/or extended opcode by matching the fetched instructions against selected opcodes. The matching may be performed through the use of one or more mask registers. A matched instruction is signified through a bit in the pre-decode information that is stored with the instruction in the instruction cache. Match bit **606** and opcode/instruction bits **608** are then stored in instruction cache **610** until selection for progress through the remainder of the instruction pipeline.

Davidson, as described above, teaches that instructions are identified by their opcode and/or extended opcode by matching the fetched instructions against selected opcodes. Davidson does not disclose, either in the above recitation, or elsewhere in the patent, that "the instruction is associated with a performance indicator stored in a shadow memory, the shadow memory comprising a storage area separate from the instruction storage area and storing performance indicators associated with instructions stored in the instruction storage area" as now recited in claim 1.

The Examiner refers to Monitor Mode Control Register (MMCR) **270** in Davidson as corresponding to the "shadow memory" recited in the claims stating that the MMCR comprises a storage area separate from an instruction area, and, therefore, can be considered as a shadow memory. The Examiner refers to col. 4, line 9 to col. 5, line 30 as describing the MMCR;

> Performance monitor **260** comprises event detection and control logic, including PMC1-PCM4 **262-268** and MMCR **270**. Performance monitor **260** is a software-accessible mechanism intended to provide detailed information with significant granularity concerning the utilization of processor instruction execution and storage control. The performance monitor may include an implementation-dependent number of performance monitor counters (PMCs) used to count processor/storage related events. These counters may also be termed "global counters". The MMCRs establish the function of the counters with each MMCR usually controlling some number of counters. The PMCs and the MMCRs are typically special purpose registers physically residing on the processor. These registers are accessible for read or write operations via special instructions for that purpose. The write operation is preferably only allowed in a privileged or supervisor state, while reading is preferably allowed in a problem state since reading the special purpose registers does not change a register's content. In a different

embodiment, these registers may be accessible by other means such as addresses in I/O space. In the preferred embodiment, PMC1-PMC4 are 32-bit counters and MMCR is a 32-bit register. One skilled in the art will appreciate that the size of the counters and the control registers are dependent upon design considerations, including the cost of manufacture, the desired functionality of processor **250**, and the chip area available within processor **250**.

Performance monitor **260** monitors the entire system and accumulates counts of events that occur as the result of processing instructions. In the present invention, processor **250** allows instructions to execute out-of-order with respect to the order in which the instructions were coded by a programmer or were ordered during program compilation by a compiler. Processor **250** also employs speculative execution to predict the outcome of conditional branches of certain instructions before the data on which the certain instructions depend is available. The MMCRs are partitioned into bit fields that allow for event/signal selection to be recorded/counted. Selection of an allowable combination of events causes the counters to operate concurrently. When the performance monitor is used in conjunction with speculatively executed instructions in the manner provided by the present invention, the performance monitor may be used as a mechanism to monitor the performance of the processor during execution of both completed instructions and speculatively executed yet uncompleted instructions.

With reference now to **FIG. 3**, an illustration provides an example representation of one configuration of an MMCR suitable for controlling the operation of two PMCs. As shown in the example, an MMCR is partitioned into a number of bit fields whose settings select events to be counted, enable performance monitor interrupts, and specify the conditions under which counting is enabled. Alternatively, an MMCR may set an initialization count value, which is not shown in the figures.

The initialization count value is both variable and software selectable. The initialization count value may be loaded into a counter when an instruction is first scheduled for execution. For example, given that the event under study is "register accesses", if the initialization count value denotes a number of register accesses for an associated instruction, then completion of the instruction allows the number of register accesses for the particular instruction to be added to the total event count in a PMC that counts all register accesses by all instructions. Of course, depending on the data instruction being executed, "complete" may have different meanings. For example, for a "load" instruction, "complete" indicates that the data associated with the instruction was received, while for a "store" instruction, "complete" indicates that the data was successfully written. A user-readable counter, e.g., PMC1, then provides software access of the total number of register accesses since PMC1 was first initialized. With the appropriate values, the performance monitor is readily suitable for use in identifying system performance characteristics.

Bits **0-4** and **18** of the MMCR in **FIG. 3** determine the scenarios under which counting is enabled. By way of example, bit zero may be a freeze counting bit such that when the bit is set, the values in the PMCs are not changed by hardware events, i.e. counting is frozen. Bits **1-4** may indicate other specific conditions under which counting is performed. Bits **5**, **16**, and **17** are utilized to control interrupt signals triggered by PMCS. Bits **6-9** may be utilized to control time or event-based transitions. Bits **19-25** may be used for event selection for PMC1, i.e. selection of signals to be counted for

> PMC1. The function and number of bits may be chosen as necessary for selection of events as needed within a particular implementation.

From the above recitation, it is clear that the MMCR is "partitioned into a number of bit fields whose settings select events to be counted, enable performance monitor interrupts, and specify the conditions under which counting is enabled". The MMCRs is a register that control the operation of the PMCs. In the present invention on the other hand, as now more clearly recited in claim 1, the shadow memory comprises a storage area that is separate from the instruction storage area and that stores performance indicators associated with instructions that are stored in the instruction storage area, and that a selected action is performed if a performance indicator (among performance indicators stored in the shadow memory) is associated with the instruction (among instructions stored in the instruction storage area). The MMCR in Davidson is not a storage area "separate from the instruction storage area and storing performance indicators associated with instructions stored in the instruction storage area", and Davidson does not disclose "performing the selected action if a performance indicator is associated with the instruction" as also recited in claim 1. Claim 1, accordingly, is not anticipated by Davidson and patentably distinguishes over Davidson in its present form.

Claims 2-7 depend from and further restrict claim 1 and are also not anticipated by Davidson, at least by virtue of their dependency. Several of these claims additionally recite subject matter that is not disclosed in Davidson. For example, claim 3 recites the manner by which a determination of being in an enabled state to perform a selected action is made, and claim 7 specifies that the shadow memory contains debugging information. Neither the subject matter of claim 3 nor the subject matter of claim 7 appears to be disclosed or suggested by Davidson. With respect to claim 7, in particular, although Davidson discloses a debugging capability in col. 7, lines 59-61, the reference does not disclose that debugging information is contained in a shadow memory. Claims 3 and 7, accordingly, are not anticipated by Davidson in their own right as well as by virtue of their dependency.

Independent claims 8, 12, 16, 19 and 23 have been amended in a manner similar to claim 1, and are also not anticipated by Davidson for similar reasons as discussed above with respect t claim 1, Claims 9-11, 13-15, 17-18, 20-22 and 24-25 depend from and further restrict one of independent claims 8, 12, 16, 19 and 23, and are also not anticipated by Davidson, at least by virtue of their dependency or as discussed above with respect to claims 3 and 7.

Therefore, the rejection of claims 1-25 under 35 U.S.C. § 102 has been overcome.

IV. Conclusion

For all the above reasons, it is respectfully urged that claims 1-25 are allowable in their present form, and that this application is now in condition for allowance. It is, accordingly, respectfully requested that the Examiner so find and issue a Notice of Allowance in due course.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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